MADANAPALLE INSTITUTE OF TECHNOLOGY & SCIENCE

(UGC-AUTONOMOUS INSTITUTION)





Examination Branch

M. Tech (VLSI Design & Embedded Systems) - I Year II Semester (R24) Regular End Semester **Examinations August-2025**

(For 2024 Admitted batch)

TIME TABLE

Academic Year: 2024-25

Time: 10:00 AM to 01:00 PM

Duration: 3 hours

DATE / DAY	Course Name & Code
04.08.2025 (Monday)	CMOS Analog IC Design-24VESP103
06.08.2025 (Wednesday)	Embedded System Design-24VESP104
11.08.2025 (Monday)	Pattern Recognition and Machine Learning-24VESP407
13.08.2025 (Wednesday)	Physical Design Automation-24VESP412

Note: (i) Any clashes or omissions in the time table may please be informed to the Controller of Examinations Immediately. (ii) Even if Government declares holiday on any of the above dates, the examination shall be conducted as usual.

Date: 04.07.20250 14 Kadiri Road Angal

Copy to:

Madanadans

1. ECE HOD

2. Transport Incharge

3. Notice Board (AS & Dept)

4. File (AS)

E Copy To: Vice Principal (Academics), Vice Principal -PG

Vice Principal (Administration)

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